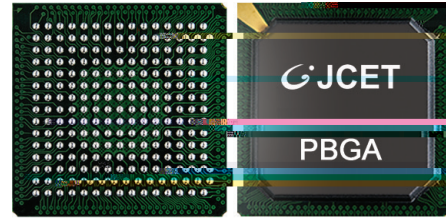


PBGA

Plastic Ball Grid Array

Highlights

- Strip molded, cost effective, high I/O package solution
- Wide range of tooled up body sizes for minimum cost of entry
- Available in Pb-free and eutectic versions



Features

- Full in-house package and substrate design capability
- Full in-house electrical, thermal and mechanical simulation and measurement capability
- Multiple metal layer options for signal, power and ground planes for improved electrical performance
- Wide range of custom and open tool designs available
- Flexible body sizes ranging from 15 x 15mm to 40 x 40mm
- 0.65, 0.80, 1.00, 1.27 and 1.50mm ball pitch with greater than 1000 I/O available
- Perimeter or full ball array
- Pb-free and green material set options
- Multiple chip design and optional passive/discrete components available (SIP)
- JEDEC standard compliant

Applications

- ASIC
- DSPs and Memory
- Gate Array
- Microprocessors/Controllers/Graphics
- PC Chipsets
- Other advanced applications requiring enhanced thermal and electrical performance

Description

BGA technology was first introduced as a solution for the increasingly high lead counts required for advanced semiconductors used in applications such as portable computers and wireless telecommunications. As the number of leads surrounding the ICs increased, high lead count packages experienced significant electrical shorting problems. BGA technology solved this problem by effectively creating leads on the bottom surface of the package in the form of small bumps or solder balls. BGA packages can be used for high performance applications with high I/O connections and high thermal and electrical requirements. The characteristics of BGA packages make them suitable for a wide variety of devices used in computing platforms, networking, hand-held consumer products, wireless communications devices, video cameras, home electronic devices and game consoles.

We offer a range of BGA packages including the Plastic Ball Grid Array (PBGA) package family. PBGA utilizes laminate substrates, and is available over a variety of standard JEDEC body sizes and ball counts to meet a wide range of customer requirements. This package provides a cost-effective advanced packaging solution, offering higher density over traditional leadframe packages.

Green and lead-free material sets are available for all PBGA package types.



Specifications

Die Thickness	150-381μm (6-15mils)
Gold Wire	15-30μm (0.6/0.7/0.8/0.9/1.0/1.1/1.2mils) diameter
Pd/Cu Wire	15-30μm (0.6/0.7/0.8/1.0mils) diameter
Bond Pad Pitch	45μm inline or 25/50μm staggered capable
Mold Cap Thickness	0.7-1.17mm
Marking	Laser
Packing Options	JEDEC tray/tape & reel

Reliability

Moisture Sensitivity Level	JEDEC Level 2A, 260°C Reflow
Temperature Cycling	-65°C to 150°C, 1000 cycles (typical)
High Temperature Storage	150°C, 1000 hrs (typical)
Pressure Cooker Test	121°C, 100% RH/2 atm, 168 hrs
Liquid Thermal Shock	(Condition B) -55°C/125°C, 1000 cycles

Thermal Performance θ_{ja} (°C/W)

Thermal performance is highly dependent on package size, die size, substrate layers and thickness, and land configuration. Simulation for specific applications should be performed to obtain maximum accuracy.

Package	Body Size (mm)	Pin Count	Die Size (mm)	Thermal Performance θ_{ja} (C/W)
27 x 27	2L	256	7.8 x 7.8	29.8
27 x 27	4L	256	7.8 x 7.8	22.4
27 x 27	4L	272	7.8 x 7.8	20.2
35 x 35	4L	388	10.2 x 10.2	15.9

Note: Simulation data for package mounted on 4 layer PCB (per JEDEC JESD51-9) under natural convection as defined in JESD51-2.

Electrical Performance

Electrical parasitic data is highly dependent on the package layout. 3D electrical simulation can be used on the specific package design to provide the best prediction of electrical behavior. First order approximations can be calculated using parasitics per unit length for the constituents of the signal path. Data below is for a frequency of 100MHz and assumes 1.0 mil gold bonding wire.

Conductor Component	Length (mm)	Resistance (mOhms)	Inductance (nH)	Inductance Mutual (nH)	Capacitance (pF)	Capacitance Mutual (pF)
Wire	2	120	1.65	0.45 - 0.85	0.10	0.01 - 0.02
Net (2L)	2 - 7	34 - 119	1.3 - 4.55	0.26 - 2.28	0.25 - 0.95	0.06 - 0.42
Total (2L)		154 - 239	2.95 - 6.2	0.71 - 3.13	0.35 - 1.05	0.07 - 0.44
Wire	2	120	1.65	0.45 - 0.85	0.10	0.01 - 0.02
Net (4L)	2 - 7	34 - 119	0.90 - 3.15	0.18 - 1.58	0.35 - 1.10	0.06 - 0.42
Total (4L)		154 - 239	2.55 - 4.80	0.63 - 2.43	0.45 - 1.20	0.07 - 0.44

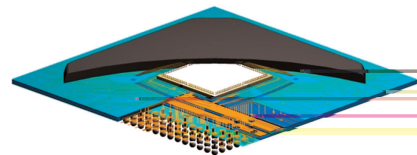
Note: Results are simulated values per JEDEC EIA/JEP123 standards.

Package Configurations

Body Size Ball Count
(mm)

15 x 15	160, 176, 196
17 x 17	192, 196, 208, 217, 252, 256
17.2 x 17.2	512
19 x 19	272, 289, 292, 296, 297, 300, 301, 305, 324, 376
21 x 21	400, 456, 484
23 x 23	169, 192, 208, 217, 233, 241, 288, 301, 304, 305, 318, 320, 324, 338, 340, 348, 352, 360, 376, 385, 388, 420, 456, 480, 484, 492
27 x 27	225, 256, 272, 277, 292, 300, 312, 316, 320, 324, 336, 352, 384, 388, 400, 416, 456, 472, 480, 484, 496, 508, 512, 544, 580, 585, 636, 650, 676
31 x 31	304, 320, 353, 385, 421, 433, 434, 448, 458, 460, 480, 540, 556, 560, 564, 604, 608, 609, 640, 644, 652, 676, 688, 692, 701, 721, 772, 896
35 x 35	304, 312, 313, 340, 352, 385, 388, 400, 420, 426, 432, 448, 452, 454, 456, 458, 474, 480, 484, 492, 496, 512, 516, 532, 542, 544, 548, 556, 564, 573, 580, 611, 624, 640, 648, 661, 665, 676, 680, 688, 700, 716, 729, 736, 740, 748, 756, 792, 816, 824, 840, 867, 868, 1012, 1156
37.5 x 37.5	435, 480, 552, 600, 601, 625, 627, 685, 701, 785, 788, 804, 840, 841
40 x 40	503, 557, 569, 596, 600, 745, 776, 928, 961, 1253

Cross Section



JCET Group Co., Ltd.

www.jcetglobal.com

The JCET logo is a registered trademark of JCET Group Co., Ltd. Trademark registered in the People's Republic of China (registration number: 3000529). All other product names and other company names herein are for identification purposes only and may be the trademarks or registered trademarks of their respective owners. This brochure as well as datasheets herein are for presentation purposes only. JCET or its subsidiaries do not warrant or make any representation whatsoever, express, implied or statutory, as to the accuracy, adequacy, reliability, completeness or otherwise. Readers are advised to seek professional advice at all time and obtain independent verification of the information contained herein before making any decision. JCET reserves the right to change the